



ABCs of ADCs

Analog-to-Digital Converter Basics

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Agenda - ABCs of ADCs

- **What's an ADC?**
- **Review of Definitions**
- **Sources of Distortion and Noise**
- **Common Design Mistakes**
- **High Speed ADCs at National**



What Is an ADC?

- **Mixed-Signal Device**
 - Analog Input
 - Digital Output
- **May be Considered to be a Divider**
 - Output says: Input is What Fraction of V_{REF} ?
- ➔ **Output = $2^n \times G \times A_{IN} / V_{REF}$**
 - n = # of Output Bits (Resolution)
 - G = Gain Factor (usually “1”)
 - A_{IN} = Analog Input Voltage (or Current)
 - V_{REF} (I_{REF}) = Reference Voltage (or Current)

Because the Analog-to-Digital Converter (A/D Converter or ADC) has both analog and digital functions, it is a mixed-signal device. Many of us consider the ADC to be a mysterious device. It can, however, be considered very simply to be the instrument that it is: a device that provides an output that digitally represents the input voltage or current level.

Notice I said **voltage** or **current**. Most ADCs convert an input voltage to a digital word, but the true definition of an ADC does include the possibility of an input current.

An ADC has an analog **reference** voltage or current against which the analog input is compared. The digital output word tells us what fraction of the reference voltage or current is the input voltage or current. So, basically, the ADC is a divider.

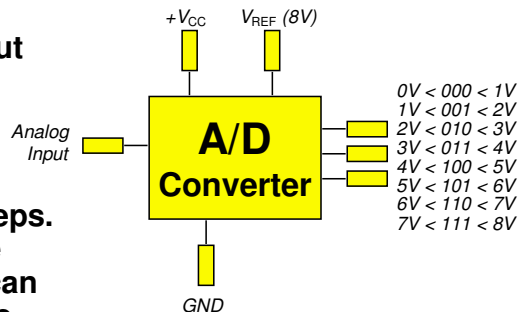
The Input/Output transfer function is given by the formula indicated here. If you have seen this formula before, you probably did not see the “G” term (gain factor). This is because we generally consider this to be unity. However, National Semiconductor has introduced ADCs with other gain factors, so it is important to understand that this factor is present.

PLEASE NOTE: The discussion here assumes an ADC with a binary output. Some of the statements here would be modified slightly for Offset Binary or 2's Complement outputs.



What, Exactly, Does An Analog-to-Digital Converter Do?

- For a 3-bit ADC, there are 8 possible output codes.
- In this example, if the input voltage is 5.5V and the reference is 8V, then the output will be 101.
- More bits give better resolution and smaller steps.
- A lower reference voltage gives smaller steps, but can be at the expense of noise.



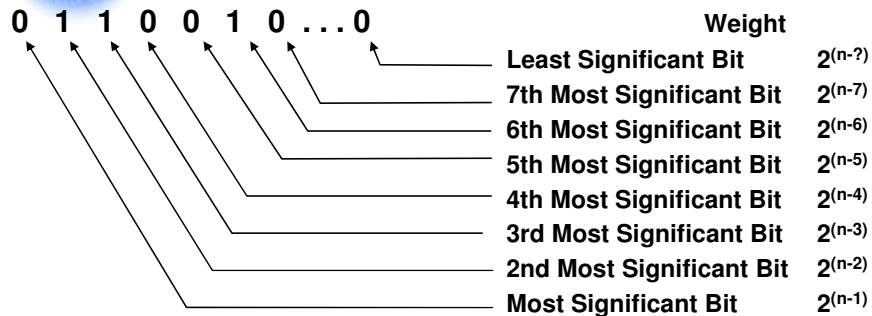
Here is an example of a 3-bit A/D converter. Because it has 3 bits, there are $2^3 = 8$ possible output codes. The difference between each output code is $V_{REF} / 2^3$.

Assuming that the output response has no errors, every time you increase the voltage at the input by 1 Volt, the output code will increase by one bit. This means, in this example, that the least significant bit (LSB) represents 1 Volt, which is the smallest increment that this converter can resolve. For this reason, we can say that the *resolution* of this converter is 1.0V because we can *resolve* voltages as small as a volt. *Resolution* may also be stated in *bits*.

Note that if you reduce the reference voltage to 0.8V, the LSB would then represent 100mV, allowing you to measure a smaller range of voltages (0 to 0.8V) with greater accuracy. This is a common way for our customers to get better precision from a converter without buying a more expensive, higher resolution converter.

The Resolution of an A/D converter is the number of output bits it has (3 bits, in this example). Resolution may also be defined as the size of the LSB (Least Significant Bit) or one count (1 Volt, in this example).

Least Significant Bit (LSB) and Most Significant Bit (MSB)



Bit Weights of an 8-Bit Word

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
128	64	32	16	8	4	2	1

The Least and Most Significant Bits (LSB and MSB) are just what their name implies: those bits that have the least weight (LSB) and most weight (MSB) in a digital word. For an n-bit word, the MSB has a weight of $2^{(n-1)} = 2^n / 2$ where "n" is the total number of bits in the word. The LSB has a weight of 1.

LSB Values by Resolution and Reference Voltage

- The value of an LSB depends upon the ADC Reference Voltage and Resolution

V_{REF}	Resolution	1 LSB
1.00V	8	3.9062 mV
1.00V	12	244.14 μ V
2.00V	8	7.8125 mV
2.00V	10	1.9531 mV
2.00V	12	488.28 μ V
2.048V	10	2.0000 mV
2.048V	12	500.00 μ V
4.00V	8	15.625 mV
4.00V	10	3.9062 mV
4.00V	12	976.56 μ V

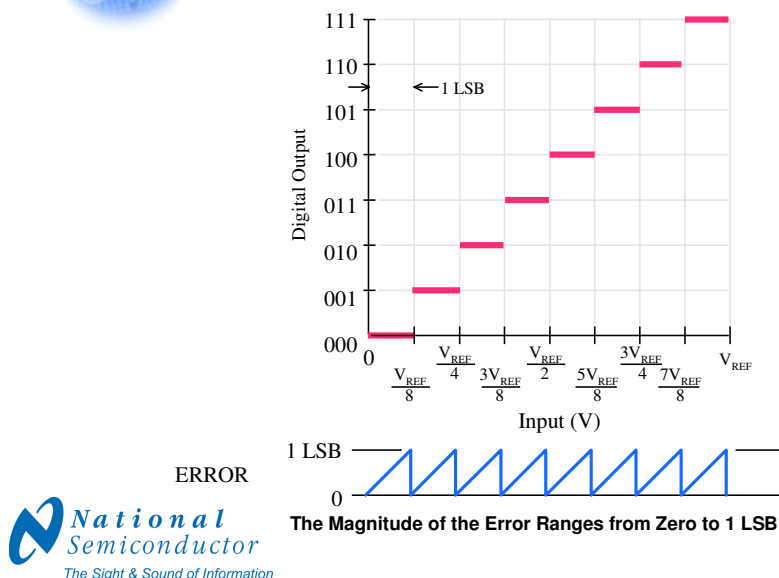
Since one LSB is equal to $V_{REF} / 2^n$, it stands to reason that better accuracy (lower error) can be realized if we did either (or both) of two things: (1) use a higher resolution converter and/or (2) use a smaller reference voltage.

The problem with higher resolution (more bits) is the cost. Also, the smaller LSB means it is difficult to find a really small signal as it becomes lost in the noise, reducing SNR performance of the converter.

The problem with reducing the reference voltage is a loss of input dynamic range. Again, we also can lose a small signal in the noise, causing a loss of SNR performance.



Quantization Error



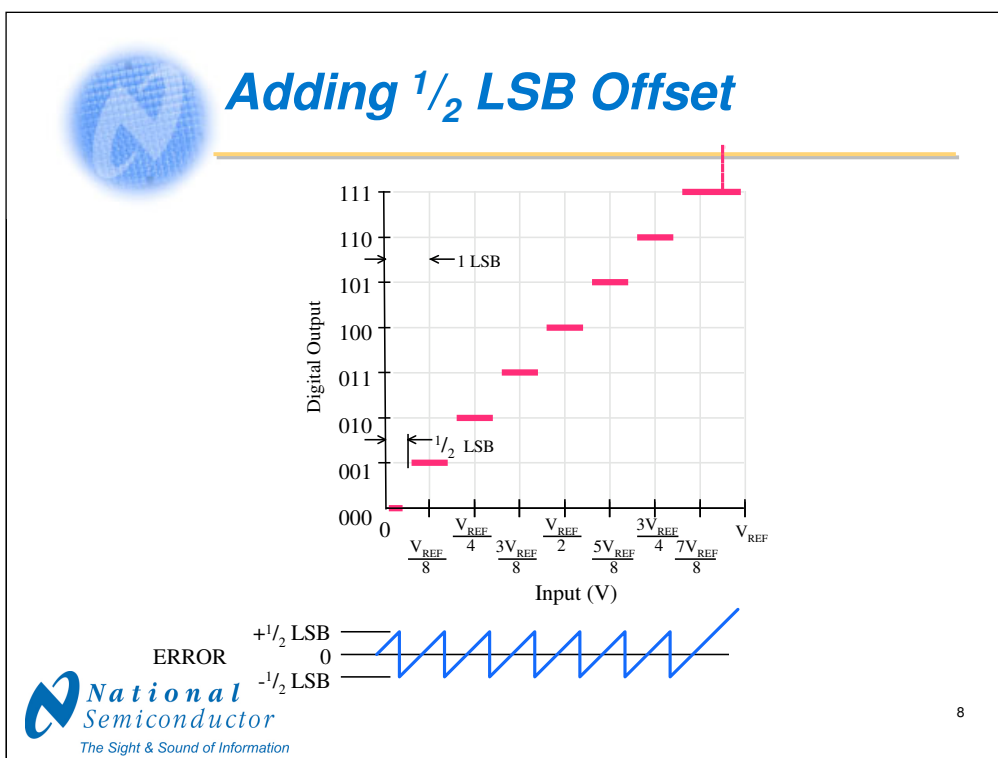
7

Continuing with the simple example of a 3-bit ADC, an ADC input of zero produces an output code of zero (000). As the input voltage increases towards $V_{REF}/8$, the error also increases because the input is no longer zero, but the output code remains at zero because a *range* of input voltages is represented by a single output code. When the input reaches $V_{REF}/8$, the output code changes from 000 to 001, where the output exactly represents the input voltage and the error reduces to zero. As the input voltage increases past $V_{REF}/8$, the error again increases until the input voltage reaches $V_{REF}/4$, where the error again drops to zero. This process continues through the entire input range and the error plot is a saw tooth, as shown here.

The maximum error we have here is 1 LSB. This 0 to 1 LSB range is known as the “quantization uncertainty” because there are a range of analog input values that could have caused any given code and we are uncertain as to exactly what the input voltage was that caused a given code. The maximum quantization uncertainty is also known as the “quantization error”. This error results from the finite resolution of the ADC. That is, the ADC can only *resolve* the input into 2^n discrete values. Each output code represents a range of input values. This range of values is a *quanta*, to which we assign the symbol q .

The converter resolution, then, is 2^n . So, for an 8 Volt reference (with a unity gain factor), a 3-bit converter *resolves* the input into $V_{REF}/8 = 8V/8 = 1$ Volt steps. Quantization error, then, is a round off error.

But an error of 0 to 1 LSB is not as desirable as is an error of $\pm 1/2$ LSB, so we introduce an offset into the A/D converter to force an error range of $\pm 1/2$ LSB.



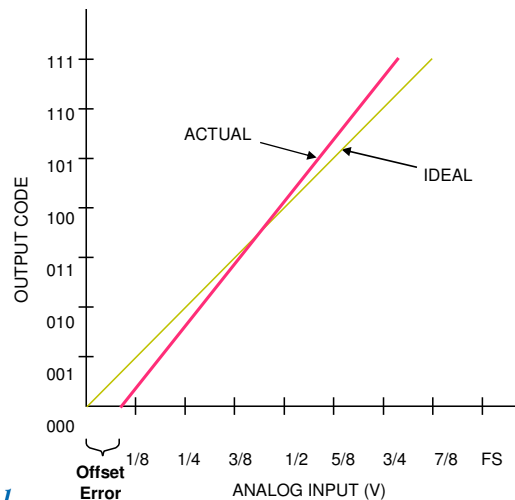
If we add $1/2$ LSB offset to the ADC input, the output code will change $1/2$ LSB before it otherwise would. The output changes from 000 to 001 with an input value of $1/2$ LSB rather than 1 LSB and all subsequent codes change at a point $1/2$ LSB below where they would have changed without the added offset.

With an input voltage of zero, the output code is zero (000), as before. As the input voltage increases towards the $1/2$ LSB level, the error increases because the input is no longer zero, but the output code remains at zero. When the input reaches $1/2$ LSB, the output code changes from 000 to 001. The input is not yet at the 1 LSB level, but only at $1/2$ LSB, so the error is now $-1/2$ LSB. As the input increases past $1/2$ LSB, the error becomes less negative, until the input reaches 1 LSB, where the error is zero. As the input increases beyond 1 LSB, the error increases until the input reaches $1 1/2$ LSB, where output code is increased by one and the sign of the error again becomes negative. This process continues through the entire input range.

Note that each code transition point decreased by $1/2$ LSB compared with the no offset of previous page, so that the first code transition (from 000 to 001) is at $+1/2$ LSB and the last code transition (from 110 to 111) is at $1 1/2$ LSB below V_{REF} . The output of the ADC should **NOT** "rotate" with an over range input as would a digital counter that is given more clock cycles than enough to cause a full count.



Offset Error

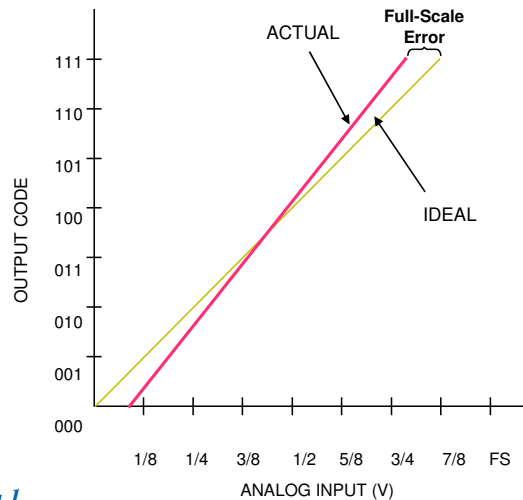


In an ideal A/D converter, an input voltage of $q/2$ will just barely cause an output code transition from zero to a count of one. Any deviation from this is called Zero Scale Error, Zero Scale Offset Error, or Offset Error. This error is positive or negative when the first transition point is higher or lower than ideal, respectively. Offset error is a constant and can easily be factored or calibrated out. Offset error may be expressed in percent of full scale voltage, Volts or in LSB.

Bottom Offset differs from Offset Error in that Bottom Offset is the input voltage required to cause a transition of the output code to the first count.



Full-Scale (Offset) Error



In an ideal A/D converter, the output code transition to full scale just barely occurs when the input voltage equals $G \cdot V_{REF} \cdot (2^n - 1.5) / 2^n$, where “G” is the gain of the converter (usually “1”), V_{REF} is the ADC reference voltage and “n” is the resolution (number of output bits) of the ADC.

In an actual ADC the full-scale analog input causing this transition may differ somewhat from this ideal value. Full Scale Error is the error in the actual full-scale output transition point from the ideal value. Part of this error will be due to offset voltage and the rest will be due to an error in the slope of the transfer function. Full Scale Error may be expressed in LSBs or as a percentage of the full-scale voltage.

Full Scale Error is sometimes called Full Scale Offset Error and is expressed in LSBs, Volts or as a percentage of ideal full scale input.

Top Offset is yet another type of full scale error, defined as the difference between the positive reference voltage and the input voltage that just causes the output code to transition to full scale plus 1.5 LSB, or V_{FS} :

$$E_{OT} = V_{FT} + 1.5 \text{ LSB} - V_{REF} = V_{FS} - V_{REF}$$

where E_{OT} is the Top Offset voltage

V_{FT} is the input voltage causing the full-scale transition

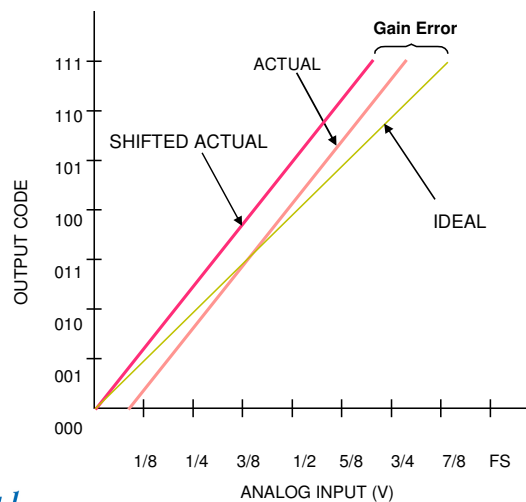
V_{REF} is the ADC reference voltage

V_{FS} is 1.5 LSB above V_{FT} .

Top Offset is a very unusual specification.



Gain Error (Full-Scale Gain Error)



Gain Error, or Full-Scale Gain Error, is a deviation from the ideal slope of the transfer function. It is the same as full-scale error with the offset error subtracted. If we shift the actual transfer curve so that zero scale offset error becomes zero, the difference between the actual and ideal transitions to full scale is the Gain Error.

Full Scale Error is expressed in LSBs, or as a percentage of the ideal full-scale voltage.



Linearity - DNL (DLE) and INL (ILE)

- **DNL - Differential Non-Linearity**
- **DLE - Differential Linearity Error**
- **INL - Integral Non-Linearity**
- **ILE - Integral Linearity Error**

DNL and DLE are the same thing and describe the error in step size. This is “small scale” code to code errors.

INL and ILE are the same thing and describe the bow in the transfer function. This is “large scale” overall transfer function error.

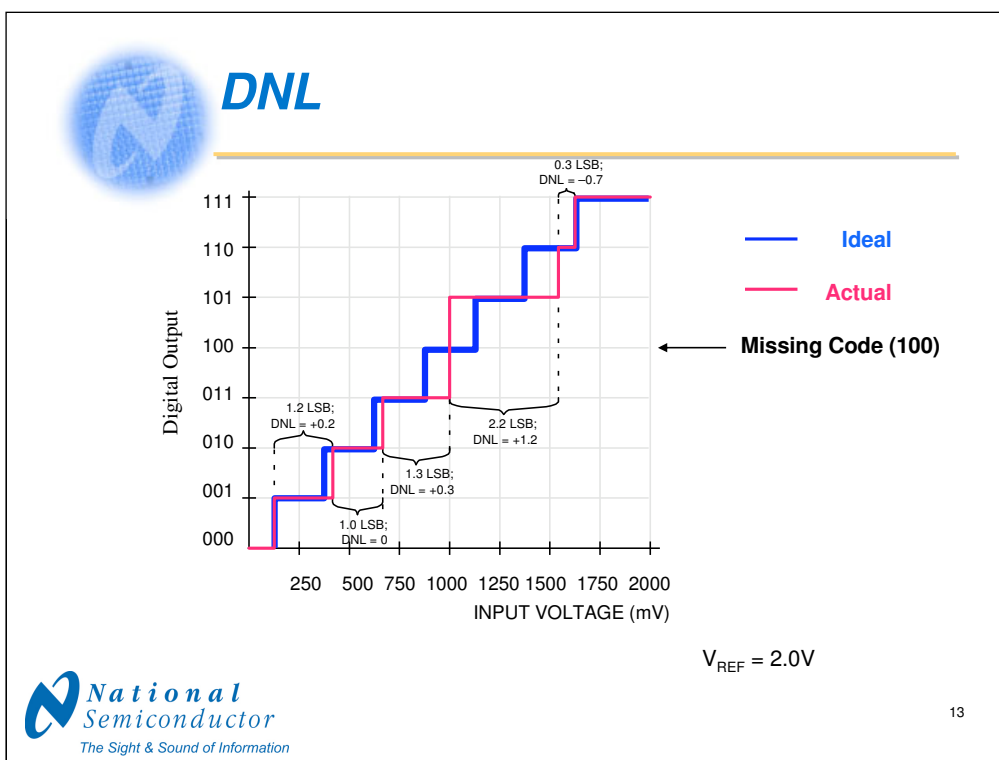


12

DNL and DLE are different terms used to describe the error in step size. Similarly, INL and ILE are different terms used to describe the maximum deviation from the ideal transfer function.

The key to remembering the difference between these two specifications is the word “Differential”. DNL is the *difference* between the ideal and the actual input code width. The input code width is the range of input values that produces the same digital output code. For positive DNL we look at the widest input code range. For negative DNL we look at the narrowest code range.

INL is the maximum deviation of the transfer function from a straight line between two points along the input-output transfer curve.



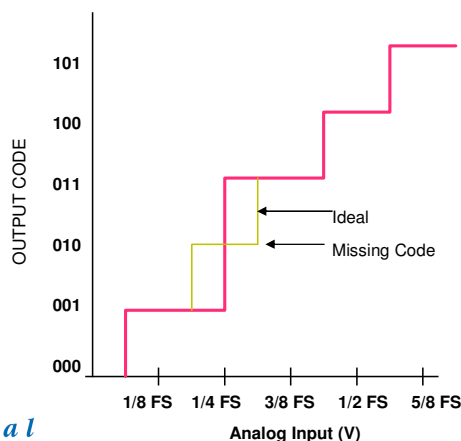
In an ideal converter, the code-to-code transition points are exactly 1 LSB apart. In an 8-bit ADC, for example, these changes are separated from each other by 1 LSB, or $1/256$ of full-scale. The difference between the ideal 1 LSB and the worst case actual input voltage change between output code transitions is called Differential Non-Linearity.

DNL can be illustrated using the transfer function of a three-bit DAC shown above. Each input step should be precisely $1/8$ of full-scale. In the example above, the first code transition (from 000 to 001) is caused by an input change of $FS / 8$ (250mV for the 2 Volt reference example shown here), where FS is the full-scale input. This is exactly as it should be. The second transition, from 001 to 010, has an input change that is 1.2 LSB, so is too large by 0.2 LSB. The input change for the third transition is exactly the right size. The digital output remains constant when the input voltage changes from 1000mV to beyond 1500mV and the code 101 can never appear at the output. It is **missing**. To avoid missing codes in the transfer function, DNL should be greater (more positive) than -1.0 LSB.

DNL indicates the deviation from the ideal 1 LSB step size of the analog input signal corresponding to a code-to-code increment. DNL, a static specification, relates to SNR, a dynamic specification. However, noise performance can not be predicted from DNL performance, except to say that SNR tends to become worse as DNL departs from zero.



Missing Codes



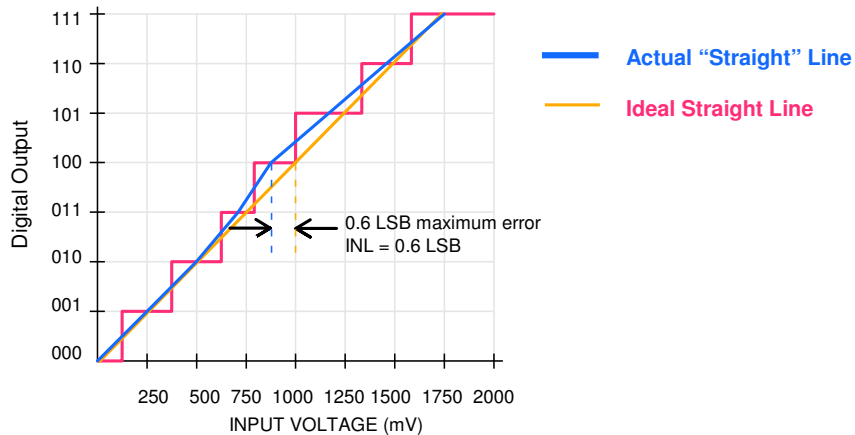
When no value of input voltage will produce a given output code, such that the code in question never appears in the output, that code is missing from the transfer function and is known as a missing code.

The transfer function above is for a three-bit A/D converter. The first code transition, from 000 to 001, takes place when the input voltage is $\frac{1}{2}$ LSB, which is correct for an A/D converter. The second transition takes place when the input voltage reaches $\frac{1}{4}$ FS, so the differential linearity error at that point is $+\frac{1}{2}$ LSB. The second transition has a differential linearity error of 1 LSB, causing the output code to jump from 001 to 011, and 010 is a Missing Code.

Any time DNL is -1.0 , there is a possibility of one or more missing codes.

Many A/D converter data sheets specify "no missing codes" as this specification can be critical in some applications, such as in servo systems.

Integral Non-Linearity (INL) or Integral Linearity Error (ILE)



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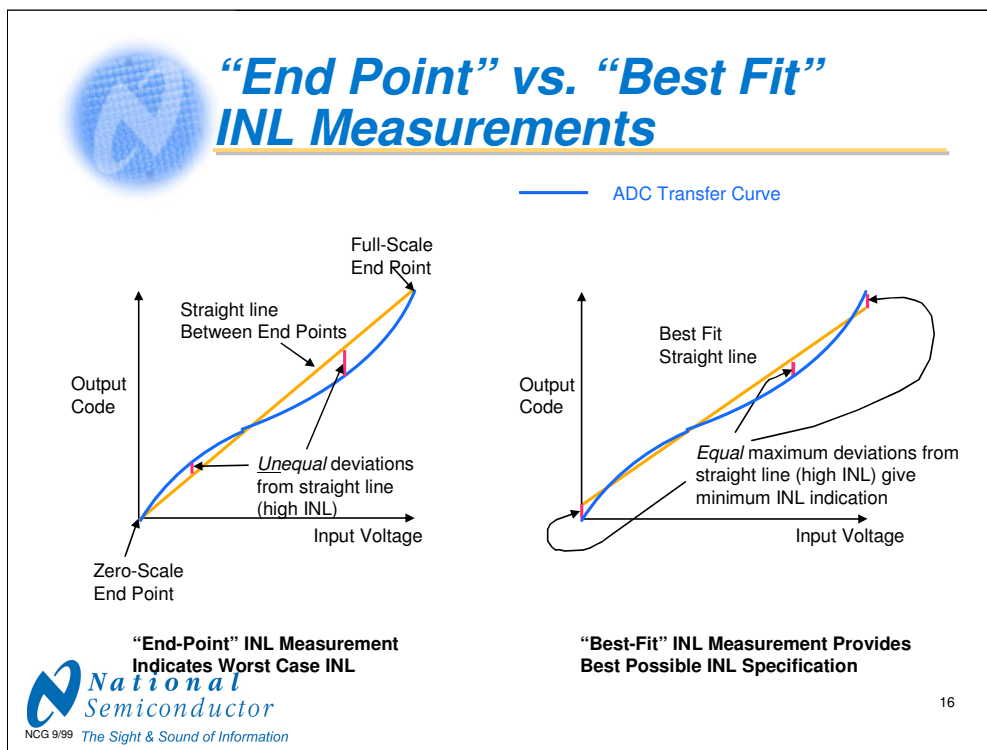
$V_{REF} = 2.0V$

15

Integral Non-linearity, INL, (also called Integral Linearity Error or ILE and Linearity Error or LE) describes the departure from an ideal linear transfer curve for an ADC (or a DAC). INL does not include quantization errors, offset error, or gain error. It is a measure of the straightness of the transfer function and can be greater than the differential non-linearity. The size and distribution of the DNL errors will determine the integral linearity of the converter.

Sometimes a converter is described as being "x bits linear." For example, a converter with 10-bit resolution and 4 LSB non-linearity is sometimes described as an "8-bit linear" converter because 4 LSBs for a 10-bit device is the same as 1 LSB for an 8-bit device.

INL is a static specification and relates to THD (a dynamic specification). However, distortion performance can not be predicted from the INL specification, except to say that THD tends to become worse as INL departs from zero.



There are two methods of measuring Integral Non-Linearity (INL):

“Best-Fit” and “End Point”. The Best-Fit measurement allows the supplier to show better INL specifications than does the End-Point INL measurement method. One argument for the Best-Fit method is that the customer can adjust his circuit to actually realize this low INL, achieving better overall performance. The problem doing this, however, is that each board must be adjusted for minimum INL for each individual converter, which is time-consuming and, therefore, expensive and not considered desirable or practical by most manufacturers.

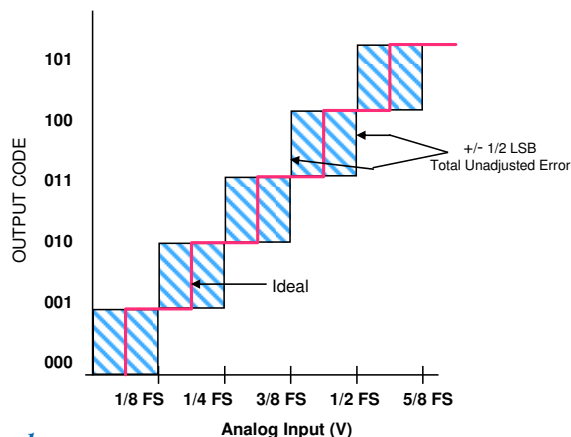
Another argument for the Best-Fit method is for dynamic applications only and says that these applications are not very concerned with offset and gain errors (which cause the End Point and Best-Fit INL methods to diverge), unless the offset and gain errors are very large, and the Best Fit method is more meaningful for these applications. This argument does indeed have some merit for dynamic applications, except they are meaningful only in that they are a better predictor of THD performance, which is usually specified anyway.

The End-Point method tells the user what worst case INL he can expect if he simply makes adjustments to his two end points. Hence, the End-Point method is seen as more practical by many. Comparing the INL of two competing devices is not reasonable when one device is measured using the end-point method and the other device uses the best-fit method because there is no correlation between the two methods.

Generally, ADCs used in d.c. applications should be have INL specified with the End Point method. It does not really matter with which method INL is specified for ADCS used in dynamic applications.



Total Unadjusted Error

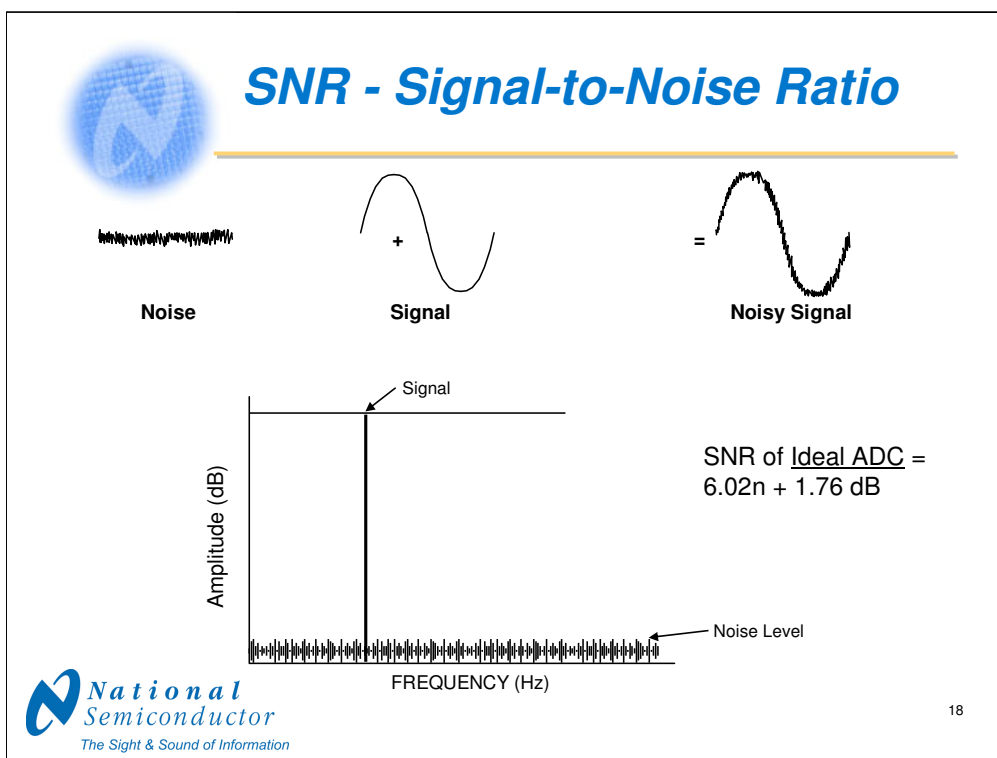


Although gain and offset errors can be trimmed externally, trimming increases costs and sometimes reduces reliability. When a designer wishes to meet a specific error budget, it is desirable to have a single specification that places a limit on errors from all sources. If this overall error limit is acceptable, no adjustments need to be made during manufacture of the end product. **Total Unadjusted Error (TUE)** is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance.

TUE is a static specification. That is, it is useful for applications with d.c. or slowly moving input signals. Such applications include, for example, digitizing the outputs of weigh scales and of temperature and pressure sensors.

You won't find this specification on all ADCs; it is of value only when the total error specification is less than one or two LSB, so it is generally not found on data sheets of converters with higher resolution than eight-bits. The ADCS7478 and the ADC121S101, for example, both are specified at ± 0.3 LSB Total Unadjusted Error while the 10- and 12-bit devices in these families do not have a TUE specification.

If the total unadjusted error is much larger than any one of the other error specifications, it makes sense to include separate data sheet limits for each of the errors. Otherwise, a device with $\pm 1/2$ LSB linearity and ± 3 LSB full-scale error might be classified simply as a "3 LSB" part and the user wouldn't know that the device could provide excellent performance in applications that require linearity but don't need full-scale accuracy.



Signal-to-Noise Ratio (SNR) is the ratio of the output signal amplitude to the output noise level, not including harmonics or dc. A signal level of $1V_{\text{RMS}}$ and a noise level of $100 V_{\text{RMS}}$ yields an SNR of 10^4 or 80dB. The noise level is integrated over half the clock frequency.

SNR usually degrades as frequency increases because the accuracy of the comparator(s) within the ADC degrades at higher input slew rates. This loss of accuracy shows up as noise at the ADC output.

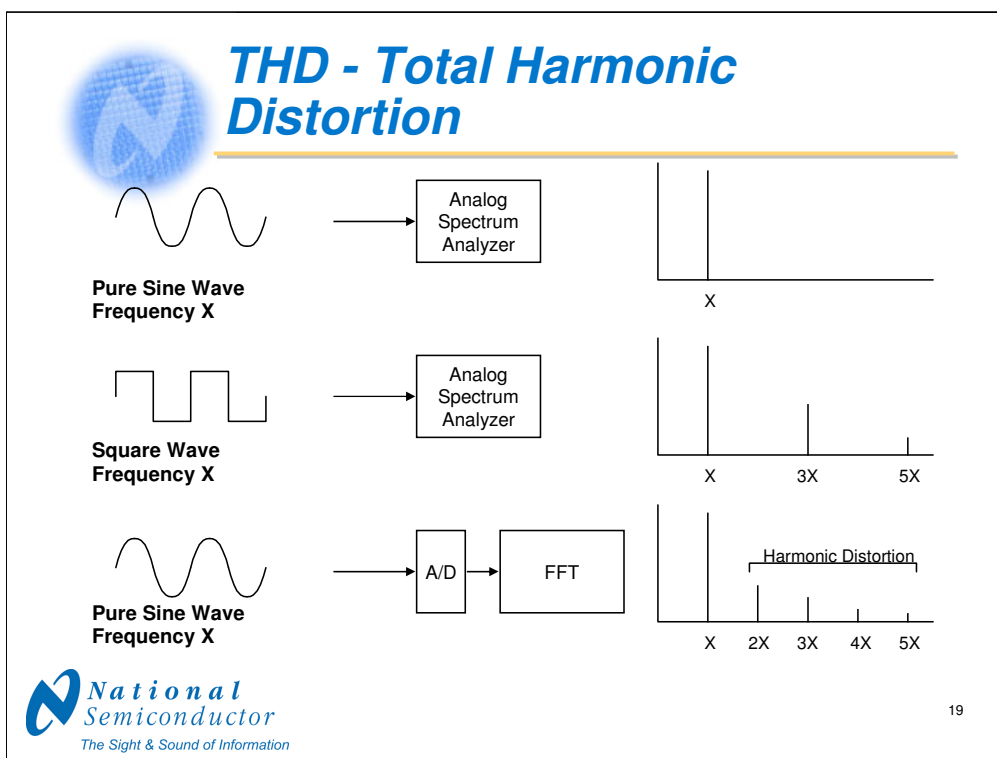
In an A/D converter, noise comes from four sources: (1) quantization noise, (2) noise generated by the converter itself, (3) application circuit noise and (4) jitter.

Quantization noise results from the quantization process--the process of assigning an output code to a range of input values. Recall our discussion on quantization error. The amplitude of the quantization noise decreases as resolution increases because the size of an LSB is smaller at higher resolutions, which reduces the maximum quantization error. The theoretical maximum signal-to-noise ratio for an ADC with a full-scale sine-wave input derives from quantization noise and is defined as $20 \cdot \log(2^{(n-1)} \times \sqrt{6})$, or about $6.02n + 1.76 \text{ dB}$.

Application circuit noise is that noise seen by the converter as a result of the way the circuit is designed and laid out. We will discuss jitter later.

SNR increases with increasing input amplitude until the input gets close to full scale. The SNR increases at the same rate as the input signal until the input signal approaches full scale. That is, increasing the input signal amplitude by 1 dB will cause a 1 dB increase in SNR. This is because the step size becomes a smaller part of the total signal amplitude as the signal amplitude increases. When the input amplitude starts approaching full scale, however, the rate of increase of SNR vs. input signal decreases.

SNR performance decreases at higher frequencies because the effects of jitter get worse, as we will see.



THD gives an indication of a circuit's linearity in terms of its effect on the harmonic content of a signal. An ideal, spectrally-pure sine wave has one frequency component. A complex signal such as music or speech has multiple frequency components. A square wave contains odd harmonics with specific amplitude and phase relationships. Ideally, a signal processing system will not add or subtract any harmonic components (unless that is the intended function of the signal processor). Non-linearities in a converter's transfer function, however, will produce harmonics that were not present in the original signal. Symmetrical non-linearities tend to produce harmonics at odd multiples of the input frequency, half wave rectification tends to produce even harmonics, while all other non-linearities tend to produce harmonics at all multiples of the input frequency.

THD is the ratio of the rms total of the first given number harmonic components to the RMS value of the output signal and relates the RMS sum of the amplitudes of the harmonics to the amplitude of the fundamental:

$$THD = \frac{\sqrt{V_{f2}^2 + V_{f3}^2 + \dots + V_{fn}^2}}{V_{f1}^2}$$

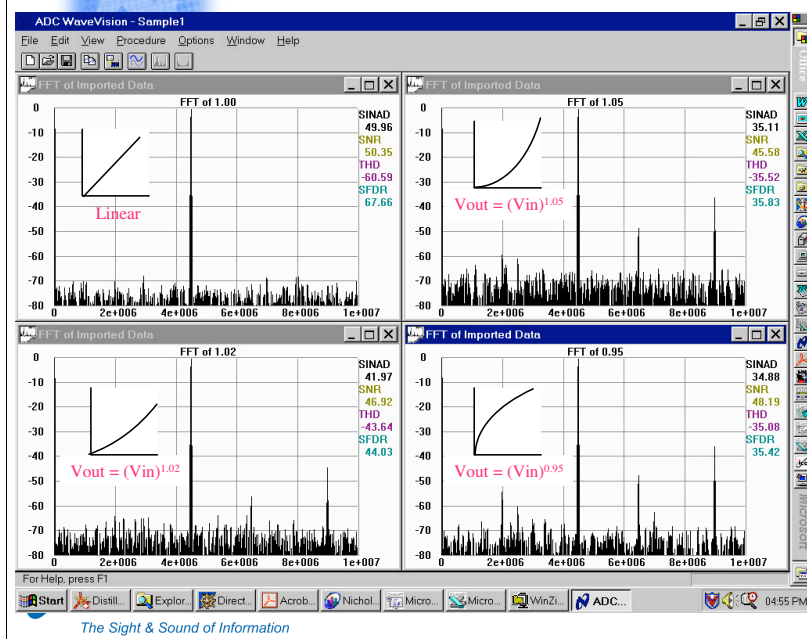
where V_{f1} is the fundamental amplitude, V_{f2} is the second harmonic amplitude, etc.

As a practical matter, there is no such thing as a completely linear input to output transfer function. This non-linearity leads to output distortion. As the input signal swing increases in amplitude, the output becomes more and more distorted. The result is an increase in distortion as the input amplitude increases.

THD performance degrades with increasing frequency because the effects of jitter get worse and because the input circuitry becomes slew limited.

THD can be expressed as a percentage or in dB.

Distortion vs.. Linearity (8 Bits)



SR = 200Mps
 fund = 45.0195 MHz
 2nd = 90.039 MHz
 3rd = 64.9415 MHz
 4th = 19.922 MHz
 5th = 25.0975 MHz
 6th = 70.117 MHz

These FFT plots, made with our WaveVision software, shows the distortion that results with different amounts and types of non-linearity.

The top left plot shows the results with a linear transfer function. All dynamic parameters are maximized.

The lower left plot is the result of an input to output transfer function of

$$\text{Output} = \text{Input}^{1.02}$$

The top right plot is the result of an input to output transfer function of

$$\text{Output} = \text{Input}^{1.05}$$

The bottom right plot results from an input to output transfer function of

$$\text{Output} = \text{Input}^{0.95}$$

At the right of the screen capture you see the harmonic frequencies. The output frequency can never be higher than $\frac{1}{2}$ the sample rate because of aliasing. Note how the harmonic amplitude increases as the exponent in the input to output transfer function departs from unity.

20



Signal-to-Noise and Distortion (SINAD)

$$\text{SINAD} = -20 * \text{Log} \sqrt{10^{\frac{-\text{SNR}}{10}} + 10^{\frac{\text{THD}}{10}}}$$

$$\text{SINAD} = 10 * \text{Log} \left[\frac{1}{10^{\frac{-\text{SNR}}{10}} + 10^{\frac{\text{THD}}{10}}} \right]$$

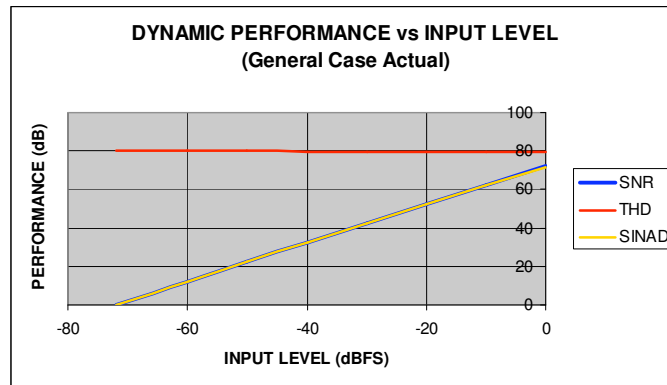
Signal-to-Noise And Distortion (SINAD) or Signal-to-Noise and Distortion Ratio (SNDR), or Signal-to-Noise Plus Distortion (S/N+D), is a combination of the SNR and the THD specifications. It is defined as the RMS value of the output signal to the RMS value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc, and can be calculated from SNR and THD according to either of the the formula here. Because it compares all undesired frequency components with the input frequency, it is an overall measure of ADC dynamic performance.

Since SINAD incorporates both SNR and THD with equal weighting, SINAD might appear to be maximum when SNR and –THD are equal to each other. However, modern ADCs exhibit such low distortion that SNR never approaches –THD very closely and SINAD tends to be maximum at or very near a full-scale input, assuming the system response is adequate.



Actual Case

- THD Much better than SNR so SINAD tracks SNR
- SINAD (and ENOB) maximum at Full Scale



The THD performance of today's ADCs is so good that it does not change much (if any at all) with input level, so SINAD is dominated by SNR, which is not as good as THD, resulting in a SINAD that closely tracks SNR.



ENOB - Effective Number Of Bits

- **ENOB says that the ADC is equivalent to this (ENOB) number of bits as far as SINAD is concerned. That is, a converter with an ENOB of 7.0 has the same SINAD as a theoretically perfect 7-bit converter.**

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

Effective Bits (also called Effective Number Of Bits, or ENOB) is a specification that helps to quantify dynamic performance. ENOB says that the converter performs as if it were a theoretically perfect converter with a resolution of ENOB. That is, an ENOB of 7.5 bits says that converter performs, as far as SINAD is concerned, as if it were an ideal 7.5-Bit ADC.

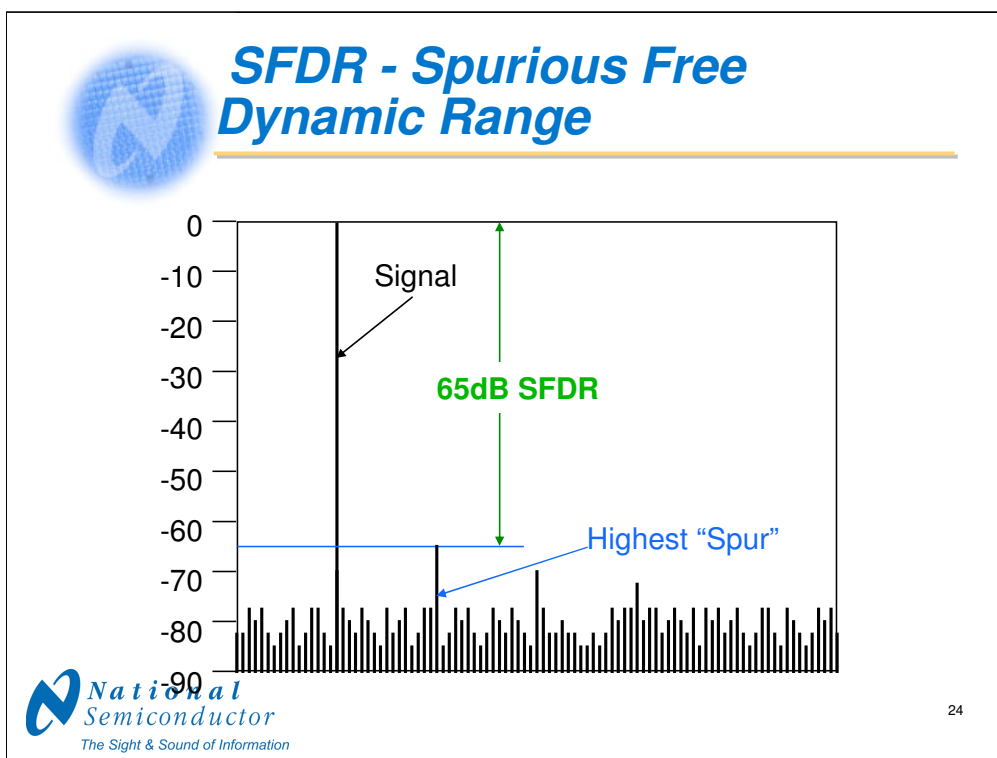
The ideal (perfect) ADC has absolutely no distortion and the only noise it exhibits is quantization noise, so SNR then equals SINAD. Since we know that SINAD for an ideal A/D converter is $(6.02n + 1.76)$ dB, we can substitute "ENOB" for "n" and calculate:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

where SINAD is expressed in dB.

So, the number of effective bits is another method of specifying SINAD. It says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

ENOB degrades as frequency increases and as input level decreases for the same reasons that THD and SNR degrade with frequency increase and improves as input level increases. Remember, ENOB comes from SINAD, which comes from THD and SNR.



Spurious Free Dynamic Range (SFDR) is the difference between the value of the desired output signal and the value of the highest amplitude output frequency that is not present in the input, expressed in dB. Some ADC suppliers ignore harmonics when specifying SFDR, but this practice is valid only if those harmonics were present at the ADC input.

Because SFDR is expressed in dB below the fundamental, it is sometimes expressed in negative dB. However, since it is a *range*, it should be expressed in positive dB.



Input Dynamic Range

Dynamic Range is the ratio of the largest to the smallest possible signals that can be resolved. DO NOT confuse with Spurious Free Dynamic Range (SFDR).

<u>Resolution (Bits)</u>	<u>Dynamic Range (dB)</u>
6	36.0
8	48.1
10	60.2
12	72.2
14	84.3
16	96.3
18	108.4
20	120.4

$$\text{Dynamic Range} = 20 * \text{Log}(2^n - 1)$$

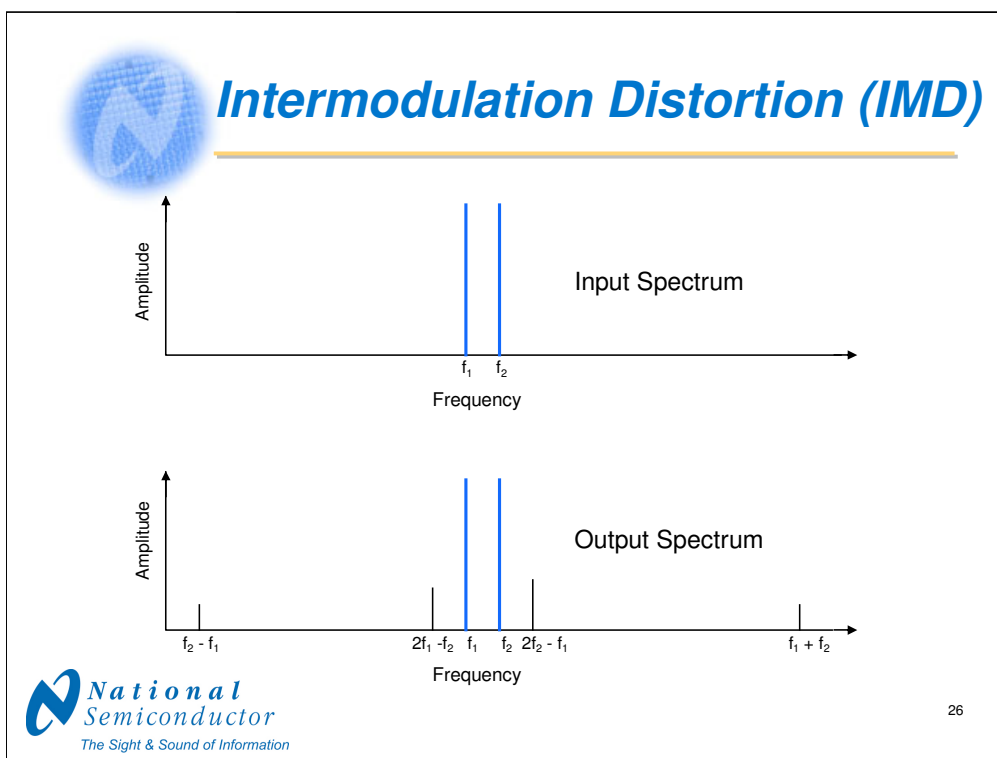


25

Input Dynamic Range (sometimes just called Dynamic Range) is the ratio of the largest to the smallest signal that can be resolved. The largest output code, of course, is $2^n - 1$ and the smallest output code, greater than 0, is 1. Dynamic range in dB, then, is

$$20 * \text{Log}((2^n - 1)/1) = 20 * \text{Log}(2^n - 1).$$

Input Dynamic Range and Spurious Free Dynamic Range (SFDR) should not be confused with each other.



Any complex signal contains components at several frequencies simultaneously. Non-linearity in the converter's transfer function will not only cause distortion of a pure tone; it will also cause two or more signal frequencies to interact with each other to produce intermodulation products. When this happens, the result is called Intermodulation Distortion, IMD.

Intermodulation distortion is measured with two or more input signals at different, closely spaced frequencies, all of the same amplitude. Two Tone IMD is the most common IMD specification and is measured with two input frequencies. Ideally, input frequencies f_1 and f_2 should produce output frequencies of only f_1 and f_2 . Device non-linearities, however, cause the production of new frequencies at the sum and difference frequencies of the input signals and their harmonics. i.e. $(f_1 + f_2)$, $(f_2 - f_1)$, $(f_1 + 2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(2f_2 - f_1)$, etc. That is, the frequencies (intermodulation products) produced are

$$\Sigma(mf_1 + nf_2)$$

where "m" and "n" can take on any integer values. The amplitudes of the various intermodulation products will depend upon the nature of the non-linearities involved.

IMD can be expressed as the ratio of the power in the intermodulation products to the power in one of the original input frequencies. Some applications, particularly those concerned with RF signal processing, are more sensitive to some modulation products than to others. For example, in RF applications the third-order difference products $(2f_1 - f_2)$ and $(2f_2 - f_1)$ are important because they are closest to the input frequencies, where other terms that are farther from the input frequencies can be digitally filtered out. For this reason the terms other than 3rd order terms are often ignored where IMD is specified for RF applications.



Sources of Noise and Distortion



Common Sources of Noise and Distortion

- **Inadequate Supply Bypassing**
- **Inadequate $V_A - V_{DR}^*$ Supply Decoupling**
- **Noisy Components/Conditioning Circuitry**
- **Quantization**
- **Clock**
- **Output to Input Coupling**

* V_{DR} (or DR V_D) is the supply for the output drivers

There are many sources of signal degradation in any analog signal chain and the circuitry associated with an ADC has its share. Many of the problem areas mentioned here are common to any analog circuitry.



Inadequate Supply Bypassing

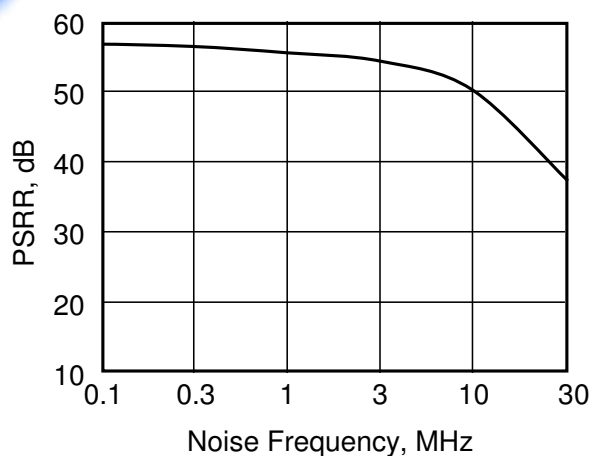
- **Noise Can Enter Via The Power Supply**
- **Specified PSRR Is A D.C. Measurement**
- **A.C. PSRR Worse Than D.C. PSRR**
- **A.C. PSRR Degrades With Frequency**

Digital circuitry typically causes a lot of noise on digital power lines. If the power source used for analog and/or mixed-signal devices is the same power source that is used for digital components, this noise can couple into the analog and mixed-signal components through their supply pins. To the extent that the analog or mixed-signal components exhibit good power supply rejection, this will not affect the analog or mixed-signal components. However, Power Supply Rejection Ratio (PSRR) degrades with increasing frequency. Furthermore, PSRR as expressed on data sheets often refers to the difference in a single parameter (e.g., Offset Voltage) with two different stable d.c. supply voltages. This says nothing about how well high frequency noise on the supply source is rejected by the component.

Noise rejection on the power supply is never quite as good as the d.c. PSRR described above and gets worse with increasing frequency.



PSRR of the ADC12040



The PSRR of the ADC12040 is excellent, yet PSRR does degrade with higher frequencies. To degrade just 8dB from 100kHz to 10MHz, however, is exceptionally good for any ADC.

This test was performed by providing a 1.2 MHz input frequency to the ADC and a.c. coupling the a constant amplitude (500 mV_{P-P}), variable frequency sine wave to the ADC power supply pins. This amplitude was measured right at the supply pins. The ADC reference was 2.0V, so if the PSRR were zero the output amplitude would have been $20 \cdot \log(0.5/2.0) = -12.04$ dBFS. The supply “noise” frequency amplitude was measured in dB. The PSRR was calculated to be the difference between this output level and 12 dB. So, for example, with 500 mV_{P-P} at 10 MHz on the supply pins,

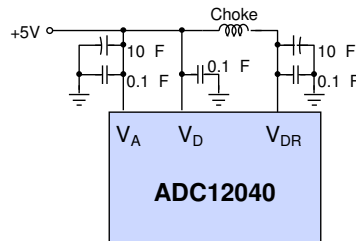
the 10MHz frequency bin was found to be at -62 dBFS, so PSRR was determined to be

$$-PSRR = -62 - (-12) = -62 + 12 = -50 \text{ dB}$$



$V_A - DR$ Decoupling

- ADC Outputs Are Digital
- Supply Current Spikes

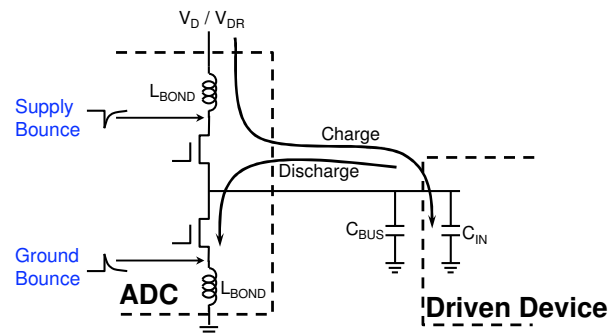


The digital output drivers of the ADC provide fairly fast edge rates (rise and fall times). This causes the output drivers to draw varying amounts of dynamic supply current with fast rise times to charge whatever capacitance is on the outputs when the output data must go from a logic low to a logic high. The noise thus introduced on the output driver supply can upset any analog circuitry if that supply is not decoupled from the ADC output drivers.

Shown here is a very good power supply decoupling technique. The very first thing to do, however, is to minimize the output bus capacitance so less current is required to charge that capacitance.



High Capacitance on ADC Outputs



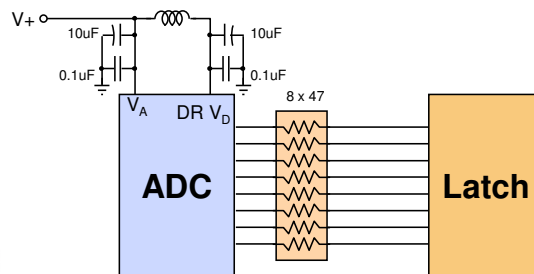
Charging bus and device input capacitances causes noise on the supply line, as we have discussed. Discharging these capacitances adds noise to the ADC substrate (die ground) and supply bus, which can appear at the input as noise. The task, then, is to minimize these currents.

Minimizing the load capacitance at the output will minimize the currents needed to charge and discharge them, lowering the noise produced by the converter itself. This implies that one output pin should drive only one input device pin (use a fan-out of one) and the length of the ADC output lines should be as short as possible.



Output to Input Coupling

- **Output “Talks” to Input**
 - Because of Output Capacitance
 - Through Substrate
- **Limiting Output Current (with Resistors) Can Help**



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33

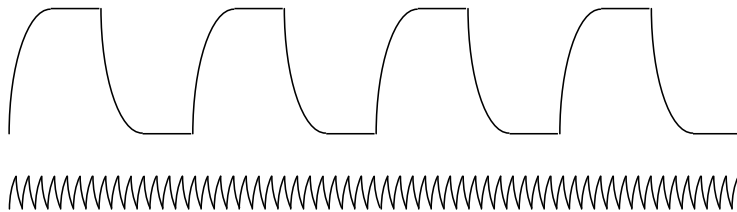
Adding series resistors in the ADC output lines will lower the current available to charge and discharge the load capacitance, lowering the noise generated on the ADC die. It is still important to minimize the load capacitance so that the RC pole is far enough out to prevent integrating the data to the point of closing the communications “eye” and the loss of signal integrity.

There is no hard and fast rule for the value of these series resistors but we have found that 100 Ohms works well for data rates up to about 50 or 60 Msps, 50 Ohms for data rates up to about 150 to 200 Msps. Above these levels, we find zero Ohms with an absolute minimization of load capacitance is necessary. Of course, these depend upon the exact layout of the circuit.



Watch the Time Constant!

- **Reduced Amplitude With Increasing Data Rate**
- **Difficulty Capturing Data**
 - **Shortened Capture Window**
 - **May Not Cross Logic Threshold**



The time constant of the series output resistors and the capacitances after those resistors form a time constant that slows the slew rate of the output. Also, that time constant reduces the output amplitude as the output data rate increases. This can make it difficult to capture the output data because the capture window is reduced. As the time constant becomes longer or the output data rate becomes faster we may find that the signal does not even cross the logic threshold and no data is captured at all.

Be careful of this time constant. At very high frequencies it may not be practical to use series resistors at the ADC output. When this is the case, it is absolutely essential to have the driven circuit very close to the ADC output pins and to use a data receiving device with a very low input capacitance.



Noisy Components/Circuitry

- **ADC Input Signal Conditioning is Common**
- **Noisy Amplifiers**
- **Resistors**
 - Noise
 - Use Low Values
- **High Frequency Coupling**
- **Resistor Packs**
 - Bandpass Characteristics
 - Oscillation
 - D.C. Offset

There is almost always a need for some signal conditioning between the stimulus source and the ADC, giving rise to a few opportunities to get noise injected into the system and to create signal distortion.

Amplifier noise is an obvious source of noise, but it is extremely difficult to find an amplifier with noise and distortion performance that will not degrade the system noise performance below that possible with a high resolution (12-bit or higher) ADC. Be very careful when choosing amplifiers and buffers in your signal conditioning circuitry.

We often think of resistors as noisy devices, but choosing resistor values that are as low as practical can keep noise to a level where system performance is not compromised.

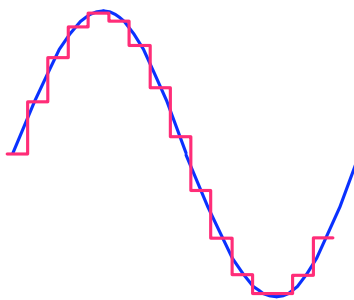
Remember that capacitive coupling of high frequency energy around some components and into unwanted areas can be a problem, so be careful with PCB (printed circuit board) layout. Part of this care should be in maintaining as linear a signal path as possible.

Resistor packs can be good for minimizing the number of components mounted or inserted and for good matching. However, the small package means there are fairly large capacitances between the individual resistors, leading to the possibility of high frequency coupling when we do not want it. These components tend to work well in digital circuitry, but can sometimes present problems in analog circuitry. Resistor packs in the input/feedback areas of an op-amp, for example, might cause a change in bandpass characteristics or encourage high frequency oscillations. Sometimes a high frequency oscillation show up as a d.c. offset.



Quantization Noise

- **Quantization Produces Noise**
- **Quantization Noise Is Inversely**
- **Inversely Proportional to ADC Resolution**



The fact that the input signal is *quantized* means that noise is added to it. Quantization noise is less with higher resolution as the input range is divided into a greater number of smaller ranges.



Clock Noise

- **Clock Can Add Noise**
- **Clock Can Be Noisy, Exhibiting Jitter**
 - For Ideal SNR, Max Jitter = $1/(2^{(n+1)} \pi f_{IN})$
- **Transmission Line**
 - Clock Line Longer Than $t_r / (6 * \text{Delay})$ Should Be Properly Terminated

The ADC clock signal can add noise to the system if proper care is not taken in its handling.

Improper routing of the clock line can cause clock noise to be coupled into the analog signal chain.

A clock signal that has cycle-to-cycle variation in its duty cycle is said to exhibit **jitter**. Clock jitter causes an uncertainty in the precise sampling time, resulting in a reduction of dynamic performance. Jitter can result from the use of a poor clock source, poor layout and grounding and from energy being coupled into the clock line from other signal sources. Sometimes you will see this formula as Max Jitter = $(V_{IN_P-P} / V_{FS}) / (2^n \pi f_{IN})$, which allows one LSB of noise. Changing 2^n to $2^{(n+1)}$ reduces the allowable noise to $1/2$ LSB and is more conservative. Changing the numerator to “1” gives us the allowable jitter for a full-scale input signal that will not degrade the signal.

The clock line should be treated as a transmission line when its length exceeds the clock rise time/(6 x Delay), where “Delay” is the propagation rate of the signal on the board, and is about 150ps/inch (6ps/mm) on a board of FR4 material. Since it is a transmission line, the clock line should be properly terminated. Other authors use factors of 4 to 5 in place of the 6 shown here, but these are marginal values. Using (6 * Delay) is more conservative and allows for variation in the dielectric constant of the board from one manufacturer to another and for layout variations.



ADC Sample Rate vs. Circuit Needs

- **Minimum Sample Rate Limitation**
- **Using an ADC Below Specified Sample Rate**
- **Getting Data Below ADC's Minimum Sample Rate**

Sometimes we can not find an ADC that is specified for the sample rate we need for a system. Usually, an ADC that is operated below its specified rate will operate at least as well at lower sampling rates. However, there are ADCs on the market (none from National Semiconductor) that will not function well if not used very close to their specified sample rate.

Most high speed ADCs have a sample rate below which they do not perform well. The reason for this is that the on-chip capacitors that must hold a charge during the conversion process are very small (to allow for the fast acquisition time required for a high speed ADC). Because they are very small, the charge on them can dissipate if the sample rate is too low. Be aware of the minimum sample rate for a converter you are using below its specified sample rate.

If you need a conversion rate below the minimum acceptable sample rate of a given ADC, simply clock it above its minimum rate and only look at every 2nd, or 3rd or 10th sample.



Common Design Mistakes

- **Inadequate Attention to Noise Minimization**
 - Ignoring PSRR
 - No Power Decoupling/Bybassing
 - Noisy Support Components
 - Excessive Clock Jitter
 - Treating Clock Line as a Trace
 - Inadequate Conditioning Circuitry
 - Inadequate Reference Driver
 - Inadequate Supply Bypassing
 - High Capacitance on ADC Outputs
- **Overdriving Any Input**

There are many possible sources of problems when using high speed ADCs, yet a surprising number of users are not aware of many of them. This leads users to use higher resolution ADCs than really needed as they try to get better noise performance or lower distortion.

We have discussed or alluded to most of these problems already. However, a word about overdriving any input and about care in driving the reference input is in order.

In addition to the possibility of exceeding the Absolute Maximum Rating of a device, driving any pin beyond the limits of the supply rails is asking for a problem unless the device is designed to handle this condition. Forcing too much current into any pin can sometimes result in a latchup condition where excessive current is drawn and the device is destroyed. This current will not go away even after the input is returned to its normal operating range, unless the power supply is interrupted. Even when the device does not latch up the device could give erroneous conversions.

Driving a pin beyond its Absolute Maximum Rating can cause device damage.



Inadequate Attention to Noise Minimization

- **Higher Resolution May Not Be The Answer**
- **Attention to PSRR and
Power Supply Decoupling**
- **Output to Input Coupling**
- **Layout and Ground Return Currents**
- **Clock Jitter**
- **Clock Line Reflections**

While using a higher resolution ADC can help improve noise performance, it is not necessarily the best solution as even this will fail to give the expected results in a poorly designed circuit. Proper attention to the other things listed here is much more effective than is a higher resolution ADC.



Noisy Components/Circuitry

- **ADC Input Signal Conditioning is Common**
- **Noisy Amplifiers**
- **Resistors**
 - Noise
 - Use Low Values
- **High Frequency Coupling**
- **Resistor Packs**
 - Bandpass Characteristics
 - Oscillation
 - D.C. Offset



41

There is almost always a need for some signal conditioning between the stimulus source and the ADC, giving rise to a few opportunities to get noise injected into the system and to create signal distortion.

Amplifiers are an obvious source of noise, but can also add distortion. The fact is, it is extremely difficult to find an amplifier with a noise and distortion performance that will not degrade the system noise performance below that possible with a high resolution (12-bit or higher) ADC. Be very careful when choosing amplifiers and buffers in your signal conditioning circuitry.

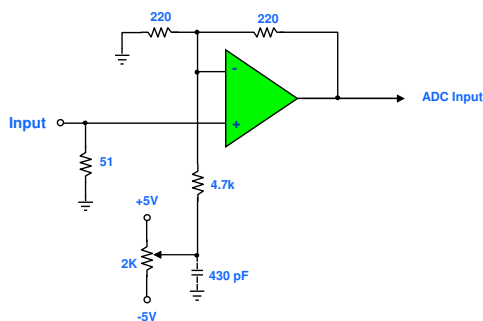
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Inadequate Conditioning Circuitry



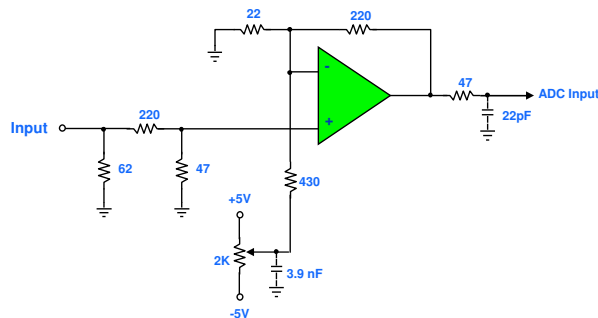
This simple circuit has a nominal gain of +2. The arm of the potentiometer is properly bypassed to prevent the gain from changing with a change of bias setting.

The problems here are two: (1) amplifiers do not like being operated at low gain settings and tend to be a little unstable when forced to do so and (2) the input of most sampling ADCs is a switched capacitor circuit, which produces current (and voltage) transients at the ADC input. Amplifiers do not like to drive such circuits. Either of these conditions lead to ringing, if not oscillation.

The 4.7k-Ohm resistor seems a little on the large side, so you might expect that it will add noise. While this value is larger than we might like to see, it probably is not as much of a problem as the low gain and the driving of the switched capacitor input of the ADC.



Better Conditioning Circuitry



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43

This is a much better solution. The amplifier is operated at a gain of about 11.5 (don't forget the effect of the 430-Ohm resistor on gain!) and the input is padded down so that the overall gain from input to output is about 2. The amplifier is happy with the high gain, but take care to watch gain bandwidth requirements.

The amplifier is decoupled from the ADC input with a simple RC. The capacitor is generally chosen such that its value is about ten times the ADC input capacitance when the ADC is in the sample or track mode, then the resistor is chosen such that the pole frequency is the sample rate. When calculating the pole frequency, be sure to include the ADC input capacitance when the ADC is in the sample or track mode. This is for converters with input frequency less than half the sample rate.

For undersampling applications, where the input frequency is higher than the sample rate, generally we do not add an input capacitor, but we do use a series resistor of about 10 to 22 Ohms.



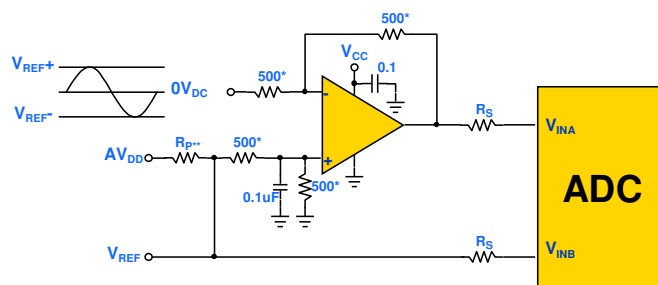
Avoid High Frequency Coupling

- **Keep Signal Path Straight**
- **Do Not Run Analog Lines Parallel to Each Other**
- **Keep Inductors Well Separated or Orthogonal to Each Other**
- **Use Care With Resistor Packs**

Avoiding problems of signal coupling requires careful attention to both capacitive coupling and mutual inductance. Very small capacitances and mutual inductances can be quite effective at coupling high frequency energy.



Resistor Pack Danger



* OPTIONAL RESISTOR NETWORK

** OPTIONAL PULL-UP RESISTOR WHEN USING INTERNAL REFERENCE



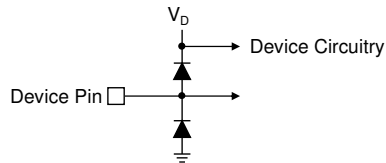
45

This innocuous-looking circuit has a hidden danger. The “optional resistor network” has some rather large capacitances that creates problems for even very slow op-amps. For example, the capacitance between the output side of the feedback resistor and the op-amp “+” input side of the two resistors connected there may cause oscillation. Sometimes the frequency of oscillation is so high it is difficult to find and we only see the results of a rectification within the amplifier or the ADC. The result is the production of an offset. If the offset is large enough, the device could be forced into a non-linear mode of operation.

Resistor packs are fine in digital applications, but be careful with them in linear circuits.



Overdriving any Input



The ESD protection diodes on the die will conduct when the input goes far enough above the supply voltage or far enough below device ground. Never assume that these diodes do not conduct until there is 600mV across them. Some of them conduct enough to be a problem with as little as 50 to 100 mV across them! As the current through these diodes become significant enough for that particular device, other parasitic diodes and transistors can be turned on. The result can be as dramatic as turning on a very low impedance path between the supply pin and ground. This is known as CMOS latchup and is destructive to the device.

A more common effect is to charge or discharge nodes within the ADC such that conversion accuracy is lost or the device may not function at all.

NEVER allow the pins of a device to go beyond the supply rails, not even on a transient basis, unless the device data sheet clearly states that it is o.k.



Clock Noise

- **Clock Can Add Noise to Conversion**
- **Clock Can Be Noisy, Exhibiting Jitter**
 - For Ideal SNR,
$$\text{Max Jitter} = V_{\text{IN(P-P)}} / (V_{\text{FS}} \times 2^{(n+1)} \times \pi \times f_{\text{IN}})$$
- **Transmission Line**
 - Clock Line Longer Than $t_r / (6 \times \text{Delay})$
Should Be Terminated

The ADC clock signal can add noise and distortion to the system if proper care is not taken in its handling.

Improper routing of the clock line can cause clock noise to be coupled into the analog signal chain.

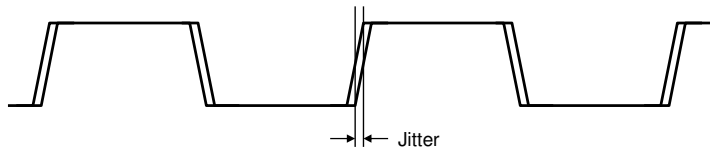
A clock signal that has cycle-to-cycle variation in its duty cycle is said to exhibit **jitter**. Clock jitter causes an uncertainty in the precise sampling time, resulting in a reduction of dynamic performance. Jitter can result from the use of a poor clock source, poor layout and grounding and from energy being coupled into the clock line from other signal sources.

The clock line should be treated as a transmission line when its length exceeds the clock rise time/(6 x Delay), where “Delay” is the propagation rate of the signal on the board, which is about 150ps/inch (60ps/cm) on a board of FR4 material.



Excessive Clock Jitter

- Time Variation of Threshold Crossing
- Caused By
 - Poor Clock Circuitry
 - Poor Layout
 - Improper Termination
 - Interference From Other Signals



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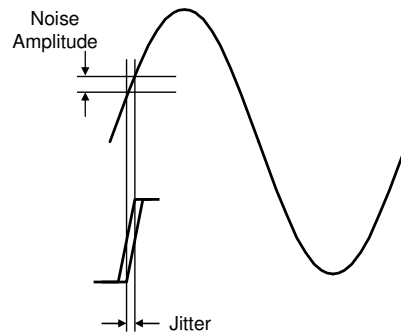
48

Jitter is the time variation of the threshold/zero crossing of a signal.

Excessive clock jitter will degrade dynamic performance of the converter.



Excessive Clock Jitter (cont'd)



$$\text{Max Jitter} = V_{\text{IN}} / (2^{(n+1)} \pi V_{\text{FS}} f_{\text{IN}})$$



49

As the clock timing changes slightly, there is a change in the exact point of sampling. This causes the ADC to sample a higher or lower point in the signal than it should. The next point could have a different time variation, so a different change from the proper sampling point. The result is a lot of variation in the signal sampling point and degraded dynamic performance of the ADC.

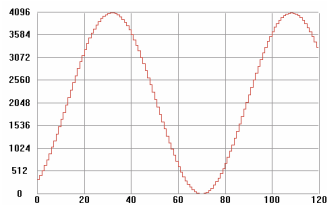
If you have seen this formula before, you may have seen it as

$$\text{Max Jitter} = 1 / (2^n \pi f_{\text{IN}}).$$

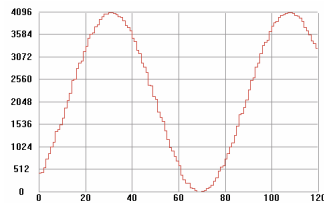
That is, with “n” rather than “(n+1)” as the exponent for the number 2. Using “n” allows for a maximum error of 1 LSB, whereas using “N + 1” allows for a maximum error of ½ LSB.



Effect of Jitter



Sampled with "clean" Clock



Sampled with Jittery Clock

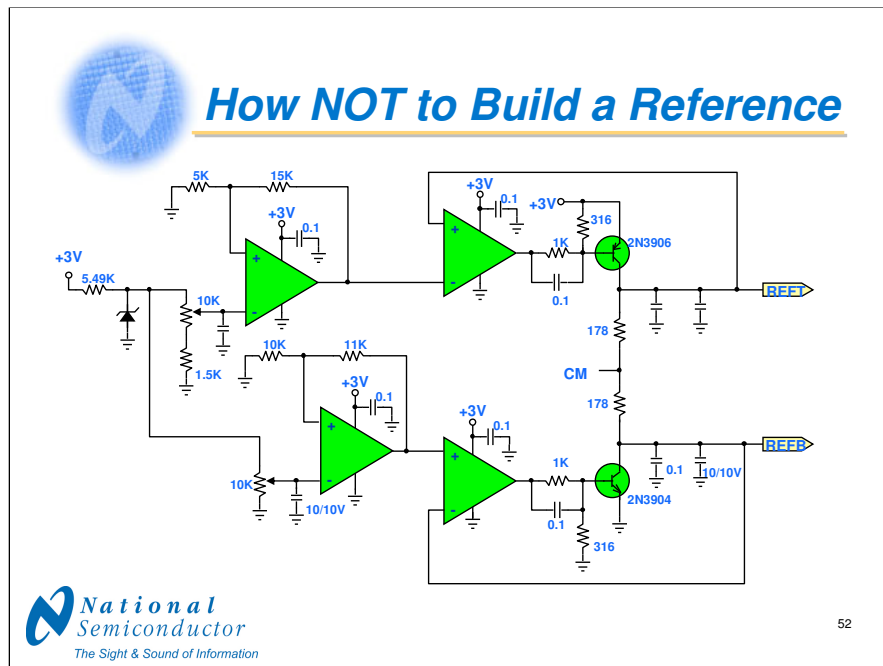
These plots from National's WaveVision software show the effects of excessive clock jitter. The noise on the signal is apparent.



Treating the Clock Line As a Trace

- **Clock Line is a Transmission Line**
 - Clock Line Longer Than $t_r / (6 * \text{Delay})$ Should Be Terminated
- **Unterminated Line Has Reflections and Standing Waves**
- **Reflections Cause Distortion**
- **Standing Waves Cause Radiation**

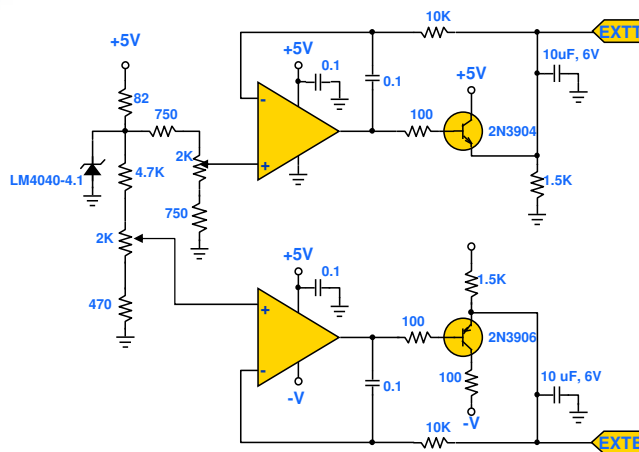
A line carrying a clock signal on a board of FR-4 material will have a typical delay of 150 ps/inch. With a 2ns rise time, a clock line longer than 2.2 inches must be considered a transmission line to maintain clock signal integrity and to minimize radiation. We suggest that you always treat the clock line as a transmission line and properly terminate it.



The problem here may not be obvious at first glance, but including the common-emitter gain of a transistor in the feedback loop of an amplifier is a recipe for high frequency oscillation. Also, this circuit has twice as many op-amps as needed and too many different resistor values, which manufacturing people really dislike!



A Better Reference Circuit



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53

This reference circuit is not only much simpler than the previous one, it is much more stable. One key factor is to choose a slow op-amp. To ensure stability, high frequency gain is killed with a 0.1uF capacitor in each op-amp feedback loop. The transistors are emitter followers, providing current gain, but no voltage gain, which could cause oscillation.

The reference circuit of many ADCs have switches connected to a resistive or capacitive ladder. These switches cause external current pulses at the reference pin(s) as they open and close. A reference drive circuit that is not capable of driving such a load and settling fast enough will result in noise on the reference pin(s), further resulting in noisy conversions. It is not necessary to eliminate these voltage spikes, but they must settle before the sampling switch opens.

A reference drive circuit that will not provide enough current to drive the ADC reference input will not be able to hold the reference stable, resulting in noisy conversions.

The circuit shown here is a good design for use as a reference driver for ADCs like the ADC1175 and ADC1175-50. Just modify the input dividers for other reference voltages for other ADCs. The potentiometers, of course, could be replaced with a fixed divider, but component tolerances must be taken into account to prevent the possibility of the input signal going beyond the resultant valid range for digitization, which would result in output clipping.



High Speed ADCs From National: 8-Bits

ADC	Res (Bits)	Speed (MSPS)	Pwr. Cons (mW)	INL (LSB)	DNL (LSB)	SNR (dB)	SINAD (dB)	SFDR (dB)	@ f _{IN} (MHz)
ADC1173	8	15	36	±0.5	±0.4	48	46	51	7.5
ADC1175	8	20	60	±0.5	±0.35	47	46	58	4.4
ADC08351	8	42	40	±0.7	±0.6	45	45	54	4.4
ADC1175-50	8	50	125	±0.8	±0.7	44	44	56	19.9
ADC08060	8	60	1.3/MSPS	±0.5	±0.4	47	47	60	25
ADC08L060	8	60	0.65/MSPS	±0.5	±0.25	47.4	46.1	54.5	29
ADC08100	8	100	1.3/MSPS	±0.5	±0.4	46.5	46	63	41
ADC08200	8	200	1.05/MSPS	+1.0 -0.3	±0.4	46	46	60	50
ADC08D500	2 x 8	500	1.4 W	±0.3	±0.15	48	47	55	248
ADC081000	8	1000	1.45 W	±0.35	±0.25	48	47	58.5	498
ADC08D1000	2 x 8	1000	1.6 W	±0.3	±0.15	47	46	55	498
ADC081500	8	1500	1.2 W	±0.3	±0.15	46	45	53	748
ADC08D1500	2 x 8	1500	1.8 W	±0.3	±0.15	46	45	53	748



* Expected specifications: product in development

54

National Semiconductor provides an increasing range of high speed ADCs. Most applications can be satisfied with a product we provide.



High Speed ADCs From National: 10-bits

ADC	Res (Bits)	Speed (MSPS)	Pwr. Cons (mW)	INL (LSB)	DNL (LSB)	SNR (dB)	SINAD (dB)	SFDR (dB)	@ f _{IN} (MHz)
ADC10321	10	20	98	±0.45	±0.35	60	59	72	4.4
ADC10D020	2 x 20	Dual 20	150	±0.65	±0.35	59	59	75	4.7
ADC10030	10	30	125	±0.45	±0.4	59	58	68	13.5
ADC10040	10	40	55.6	±0.3	±0.3	59.6	59.4	80	19
ADC10D040	2 x 40	Dual 40	267	±0.65	±0.35	60	59	72	10.4
ADC10065	10	65	68.6	±0.3	±0.3	59.3	59	80	32
ADC10080	10	80	78.6	±0.5	±0.25	59.2	59	78.8	39



High Speed ADCs From National: 12-bits

ADC	Res (Bits)	Speed (MSPS)	Pwr. Cons (mW)	INL (LSB)	DNL (LSB)	SNR (dB)	SINAD (dB)	SFDR (dB)	@ f_{IN} (MHz)
ADC12010	12	10	160	± 0.5	± 0.3	70	69	83	10
ADC12020	12	20	185	± 0.55	± 0.4	70	69	85	10
ADC12040	12	40	340	± 0.7	± 0.4	69.5	69	84	10
ADC12D040	2 x 12	40	600	± 0.7	± 0.4	68	68	80	10
ADC12DL040	12	40	210	± 0.8	± 0.3	69	69	4	20
ADC12L063	12	62	354	± 1.0	± 0.5	66	65	78	10
ADC12QS065	4 x 12	65	800	± 0.6	± 0.3	68	68	80	33
ADC12L066	12	66	357	± 1.2	± 0.4	65	64	73	25
ADC12DL066	2 x 12	66	686	± 1.2	± 0.5	64	63	72	33
CLC5957	12	70	640	± 1.5	± 0.65	66	-	74	25
ADC12L080	12	80	425	± 1.2	$\pm 0.4^*$	65	64	74	70
ADC12DL080	12	80	447	± 0.9	± 0.4	67	66	81	200



* Expected specifications: product in development

56



High Speed ADCs From National: 14 & 16-bits

ADC	Res (Bits)	Speed (MSPS)	Pwr. Cons (mW)	INL (LSB)	DNL (LSB)	SNR (dB)	SINAD (dB)	SFDR (dB)	@ f _{IN} (MHz)
ADC14L020	14	20	150	±1.4	±0.5	74	74	93	10
ADC14L040	14	40	235	±1.5	±0.5	73	73	90	20
ADC14155 *	14	155	974 *	±1.5 *	±0.5 *	71 *	71 *	85 *	70
ADC16061	16	2.5	390	±3.0	±1.0	80	79	91	0.5

* Target specifications: product in development



General Purpose ADCs From National – Guaranteed Speed Ranges

ADC	Res (Bits)	Mux Inputs	Speed (ksps)	Pwr. Cons (mW)	ADC	Res (Bits)	Mux Inputs	Speed (ksps)	Pwr. Cons (mW)
ADC081S021	8	1	50 - 200	1.3	ADC084S021	8	4	50 - 200	1.6
ADC081S051			200 - 500	1.6	ADC084S051			200 - 500	2.2
ADC081S101			500-1,000	20	ADC084S101			500 - 1,000	3.2
ADC101S021	10	1	50 - 200	1.3	ADC104S021	10	4	50 - 200	1.6
ADC101S051			200 - 500	1.6	ADC104S051			200 - 500	2.2
ADC101S101			500 - 1,000	20	ADC104S101			500 - 1,000	3.2
ADC121S021	12	1	50 - 200	1.3	ADC124S021	12	4	50 - 200	1.6
ADC121S051			200 - 500	1.6	ADC124S051			200 - 500	2.2
ADC121S101			500-1,000	20	ADC124S101			500 - 1,000	3.2
ADC082S021	8	2	50 - 200	1.6	ADC088S022	8	8	50 - 200	0.9
ADC082S051			200-500	2.2	ADC088S052			200 - 500	1.2
ADC082S101			500 - 1,000	3.2	ADC088S102			500 - 1,000	1.8
ADC102S021	10	2	50 - 200	1.6	ADC108S022	10	8	50 - 200	1.1
ADC102S051			200 - 500	2.2	ADC108S052			200 - 500	1.5
ADC102S101			500 - 1,000	3.2	ADC108S102			500 - 1,000	2.1
ADC122S021	12	2	50 - 200	1.6	ADC128S022	12	8	50 - 200	1.2
ADC122S051			200 - 500	2.2	ADC128S052			200 - 500	1.6
ADC122S101			500 - 1,000	3.2	ADC128S102			500 - 1,000	2.3



58

The groupings here are by pin compatibility. All of these devices are communicated with in the same way. This makes portability of design across resolution, speed, sample rate and multiplexor options very simple.



Other General Purpose ADCs From National

ADC	Res (Bits)	Mux Inputs	Speed (ksps)	Pwr. Cons (mW)	SE / DIFF
ADCS7476	8	1	1,000	2	SE
ADCS7477	10	1	1,000	2	SE
ADCS7476	12	1	1,000	2	SE
ADC78H89	12	7	500	1.5	SE
ADC78H90	12	8	500	1.5	SE
ADC121S625	12	1	50 to 200	1.25	DIFF



Summary - ABCs of ADCs

- **The ADC**
- **Review of Definitions**
- **Sources of Distortion and Noise**
- **Common Design Mistakes**
- **ADCs from National Semiconductor**



60

We have discussed the Analog-to-Digital Converter and its specifications. We talked about problem sources and how to get around them and ended up with a summary of National Semiconductor's high speed ADC offering.



ADC Web Site

- **Site:** www.national.com/appinfo/adc
 - shortcut: www.national.com/adc
 - shorter cut: www.nsc.com/adc
- **Link to Selection Guides**
 - General Purpose/Industrial
 - High Speed
- **Reference Material**
 - Application Notes
 - Articles
- **Evaluation Board Material**
 - Eval Board Descriptions
 - Manuals
 - WaveVision Software Download
- **Competitive Cross Reference**



62



Glossary of Terms

Absolute maximum Ratings – Voltages and currents beyond which a device may not be stressed without danger of damaging or destroying the device. The device is NOT guaranteed to work when stressed at or near its absolute maximum ratings..

A/D – See ADC.

A/D Converter – See ADC.

A.C. Termination – Transmission line termination technique where a series RC is used at the receiving end of a transmission line.

A.C. Termination – Transmission line termination technique where a series RC is used at the receiving end of a transmission line.

ADC – Analog-to-Digital Converter. A device or circuit used to convert analog information to digital words.

ADC10D040 – A 10-bit, 40 Msps (Megasample per second) ADC

ADC12040 – A 12-bit, 40 Msps (Megasample per second) ADC

ADC14080 – A 14-bit, 80 Msps (Megasample per second) ADC

Aliasing – Conversion of an input frequency to another frequency as a result of the conversion process. The output frequency of an ADC can never exceed $\frac{1}{2}$ the sampling frequency of the ADC without this aliasing. When the input frequency does exceed $\frac{1}{2}$ the sampling frequency, the output frequency becomes the absolute value of $[\text{INT}(f_{\text{IN}}/f_{\text{S}} + 0.5)] * f_{\text{S}} - f_{\text{IN}}$.

Characteristic Impedance - The impedance a transmission line such that, when driven by a circuit with that output impedance, the line appears to be of infinite length such that it will have no standing waves, no reflections from the end and a constant ratio of voltage to current at a given frequency at every point on the line.

DAC – Digital-to-Analog Converter. A device or circuit used to convert digital words into analog voltages or currents.

Director – The shorter elements of a “Yagi” antenna that directs energy toward the driven element.

DLE – Differential Linearity Error. Same as DNL.

DNL – Differential Non-Linearity. The measure of the maximum deviation from the ideal step size of 1.00 LSB.

ENOB – Effective Number Of Bits. A specification that helps to quantify dynamic performance. ENOB says that the converter performs as if it were a theoretically perfect converter with a resolution of ENOB. That is, an ENOB of 7.4 says that the converter performs, as far as SINAD is concerned, as if it were a perfectly ideal ADC with a resolution of 7.4 bits (assuming you could have fractional bits). The idea behind ENOB comes from the fact that the absolutely perfect ADC has an SNR that comes only from quantization noise and has absolutely no distortion. When this is the case, SINAD is then equal to SNR. Since SNR of the absolutely perfect ADC is $\text{SNR} = 6.02 * n + 1.76$, where “n” is the number of ADC output data bits, $\text{SINAD} = \text{SNR}$ for a perfect converter, so $\text{SINAD} = 6.02 * n + 1.76$ and $n = (\text{SINAD} - 1.76) / 6.02$ and we say that $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$.

FFT – Fast Fourier Transform. The FFT is a mathematical operation that converts signals between the time and frequency domains. We generally call the frequency domain (amplitude vs.. frequency) plot an FFT.

EMI/RFI – Electromagnetic Interference/Radio Frequency Interference. This is the radiation of EM (electromagnetic) energy that may interfere with other circuits and systems.

FR-4 – A glass epoxy printed circuit board material of woven glass cloth construction laminate with an epoxy resin binder.

Full-Scale Input Swing – The difference between the maximum and minimum input voltages that will produce a valid ADC output without going over- or under-range.

Gain Error - The error in the slope of the ADC transfer characteristic. It is the difference in the actual and ideal full scale input range values.

IMD – Intermodulation Distortion. This is the creation of new spectral components that result from two or more input frequencies modulating each other when the circuit is nonlinear.

ILE – Integral Linearity Error. This is the same as INL.

INL – Integral Non-Linearity. The maximum departure of the ADC transfer curve from the ideal transfer curve. INL is a measure of how straight is the transfer function curve. There are two popular methods of measuring INL: End Point and Best Fit. The End-Point method is the most conservative, while the Best Fit method gives lower (better-looking) values. National uses the End Point method.

Input Dynamic Range – For an ADC, the range of voltages that can be applied to the input without going under or over range.

Input Offset – The difference between the input value of 1.0 LSB and the input voltage that causes the ADC output code to transition from zero to the first code.

Input Offset Error – The difference between the ideal input value of 0.5 LSB and the input voltage that causes the ADC output code to transition from zero to the first code.

Jitter – The variation in the timing of a signal’s rising or falling edge. It can be specified as cycle-to-cycle or long term.

Loop Area – The area between the conductors of outgoing and return currents.

LSB – Least Significant Bit. The bit that has the least weight.

Missing Codes – Those ADC codes that never appear at the ADC output. These codes can not be obtained with any input value.



Glossary of Terms

Nyquist Rate – The minimum sampling rate (or frequency) needed to prevent frequency aliasing.

Nyquist Frequency – The maximum input frequency beyond which frequency aliasing results.

Offset Error – This is the same as Input Offset Error.

PC Board – Printed Circuit Board.

PCB – Printed Circuit Board.

Proximity Effect – The phenomenon whereby outgoing and return currents want to flow close to each other.

PSRR – Power Supply Rejection Ratio. A measure of how well a circuit rejects a signal on its power supply. There are two ways to specify PSRR, the most common of which is to specify the change in one parameter when the d.c. value of the power supply is changed. That is, one value of d.c. voltage is applied to the supply pins and the selected parameter (e.g. offset error) is measured. Then another d.c. voltage is applied to the supply pins and the same parameter is again measured. The extent to which the selected parameter does not change when the supply voltage is changed is the d.c. PSRR. This tells us nothing about how well an a.c. signal, such as noise, on the supply line will be rejected by the device.

The other method is to specify how an a.c. signal on the power supply will affect the output of the device. National specifies both methods for most of our ADCs. This provides the all-important a.c. PSRR, but also provides d.c. PSRR that may be compared with competition. Note, however, that the two readings have no relationship to each other.

Quantization – The process of dividing a range of analog voltages or currents into smaller “quanta” (smaller range of voltages or currents) such that each quanta is represented by a single digital code.

Quantization Error – The error introduced as a result of the quantization process. The amount of this error is a function of the resolution of the quantizer. By definition, the quantization error of an ADC is $\frac{1}{2}$ LSB.

Quantization Noise – The noise at the ADC output that is caused by the quantization process. It is defined as $20 \cdot \log(2^{(n-1)} \cdot \sqrt{6})$, or about $6.02 \cdot n + 1.76$ dB, where “n” is the number of output bits of the ADC.

Quantizer – A circuit that carries out the quantization process. Another name for an Analog-to-Digital Converter.

Reference Voltage – For an ADC, the reference voltage is the voltage against which the analog input or an ADC is compared to determine the ADC output code. For a DAC, the reference voltage is multiplied with the ratio of the DAC input code to its (full-scale code + 1) to determine its analog output.

Reflector – The longer elements of a “Yagi” antenna that reflect energy back to the driven element.

Resolution – A measure of how well the ADC input is “resolved”, or how well the value of an LSB represents the analog input. Resolution is usually expressed in bits, and then indicates the number of bits available in the ADC output word.

The number of discrete output states or values of an ADC or a DAC, Can also be expressed in the number of digital bits in the output (for ADCs) or the input (for DACs).

Sampling Noise – The inherent noise of an ADC that comes from the steps in the transfer function.

Scale Factor – The effective multiplier of the analog reference voltage input to an ADC or DAC. This value is usually one, but can be any whole or fractional number.

Series Termination - Adding a resistor in series with a transmission line such that the driver output impedance plus the resistance of this external resistor is equal to the characteristic impedance of the transmission line.

S/(N+D) – Signal-to-Noise Plus Distortion. See SINAD.

SINAD – Signal-to-Noise And Distortion ratio. A combination of the SNR and THD specifications, SINAD is defined as the rms value of the fundamental signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c. SINAD can be calculated from SNR and THD. Because it compares all undesired frequency components at the output with desired frequency. It is an overall measure of the dynamic performance of the ADC. SINAD is also known as SNDR, S/(N+D) and Signal-to-Noise Plus Distortion.

Skin Effect – The phenomenon by which high frequency current flow is restricted to the surface, or skin, of a conductor.

SNDR – Signal-to-Noise And Distortion Ratio. See SINAD.

SNR – Signal-to-Noise Ratio. The ratio of the power in the signal to the power in all other spectral components below $\frac{1}{2}$ the sampling frequency, excluding harmonics and d.c.

Split Ground Plane – Concept where analog and digital grounds are in a single PCB layer and only connected at a single point.

Substrate – The base semiconductor material upon which solid state devices are built. The substrate is resistive with a resistance that is on the order of a few Ohms.

THD – Total Harmonic Distortion. The ratio of the rms total of a specified number of harmonic components to the rms value of the output signal. National uses the first nine harmonics (f_2 through f_{10}).

Through Hole – The hole that goes through a printed circuit board to connect together lines and/or planes in two or more layers

V_{REF} – See “Reference Voltage”.

Z₀ – The characteristic impedance of a transmission line